Quin Systems Limited

CPU20 Hardware Manual

Revision 1

February 1992

(MAN509)

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Hardware Issue

This manual reflects the Issue B CPU20 hardware.

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1. Introduction

This document describes the Quin Systems CPU20 single board computer.

The CPU20 module is a low cost, low power, medium performance 32-bit processor module, based around the Motorola 68020 processor. It is designed specifically for standalone operation in rom-based embedded systems, and supports the OS-9/68020 operating system. It offers a flexible memory array which is nevertheless simple to configure, and a useful set of input/output devices. In particular, it provides access to Ethernet networks by means of the onboard ILACC local area network controller.

The CPU20 memory array is divided into three banks of four 32-pin JEDEC sockets, allowing a maximum of 12 Mbytes of memory (using hybrid devices). Each bank is configured separately for use with eprom, static ram (with optional battery backup), or eeprom. A standard configuration suitable for use with OS-9/68020 includes 1 Mbyte of eprom ($4 \times 256k \times 8$) and 1 Mbyte of static ram ($8 \times 128k \times 8$).

Two serial ports are provided by means of a standard 68681 compatible DUART device. Each port may be configured separately for RS-232 or RS-422/485 operation. A Z8536 device provides up to 20 digital input/ output lines at LSTTL levels, and up to three counter/timers. A calendar/ clock device with battery backup provides date/time information. Two hexadecimal LED displays are available for use by application software, and a hardware watchdog timer is also available.

The Ethernet interface provides access to local area networks. It may be used with the onboard “thin” Ethernet transceiver, or with an external transceiver for connection to other media such as “thick” Ethernet or twisted pair cable. Full software support is provided under OS-9/68020 for TCP/IP protocols and the Telnet and FTP programs, with optional support for Microware’s Unibridge development software and for the NFS Network File System. This makes the CPU20 ideal for use with Unix workstations, either in development or in distributed applications.

Offboard expansion is available via the G64 bus, which supports a wide range of third party input/output modules. Higher speed expansion is available via a daughter board interface for custom hardware.

2. Address Map

2.1 Memory Address Map

The address map for the CPU20 procesor module is shown below.

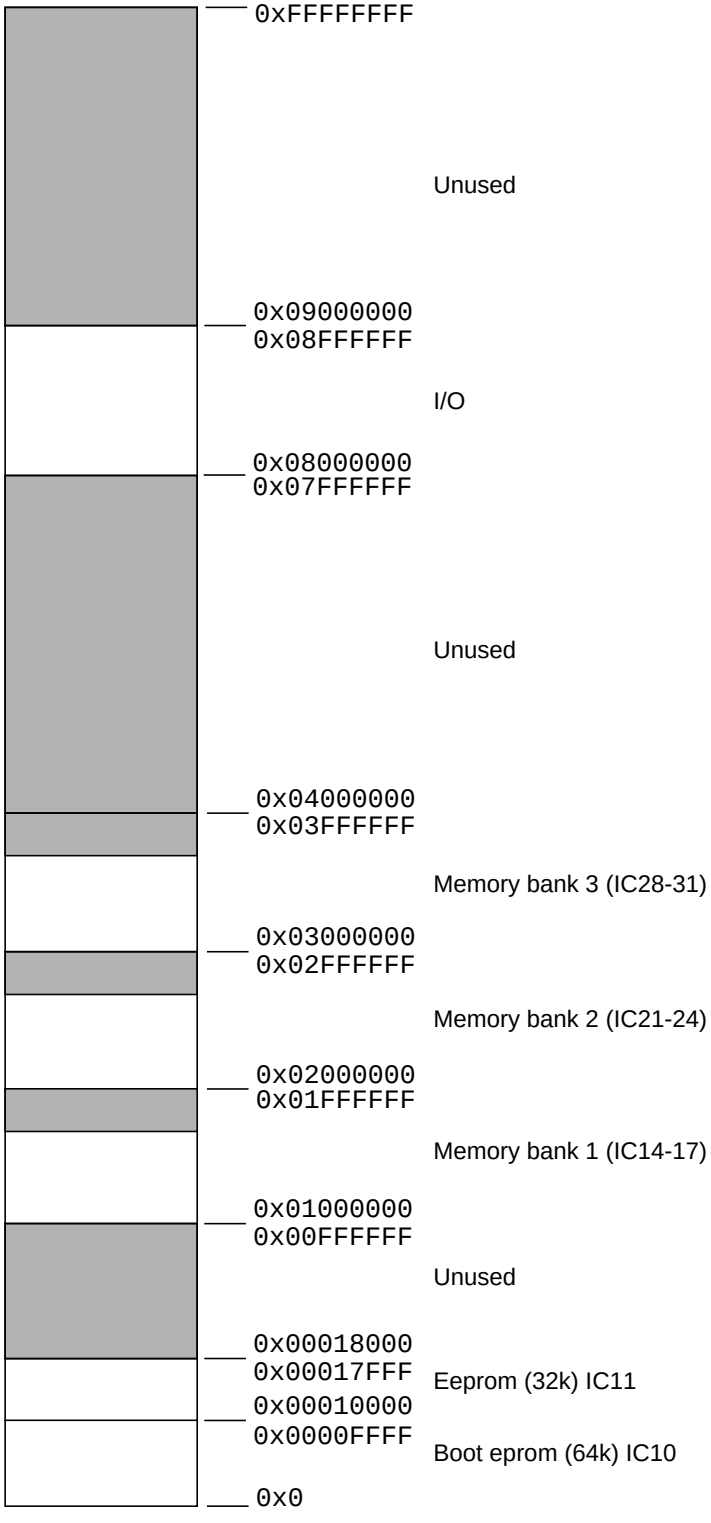


Figure 1. Address Map

2.2 I/O Address Map

The address map for the CPU20 I/O space is shown below.

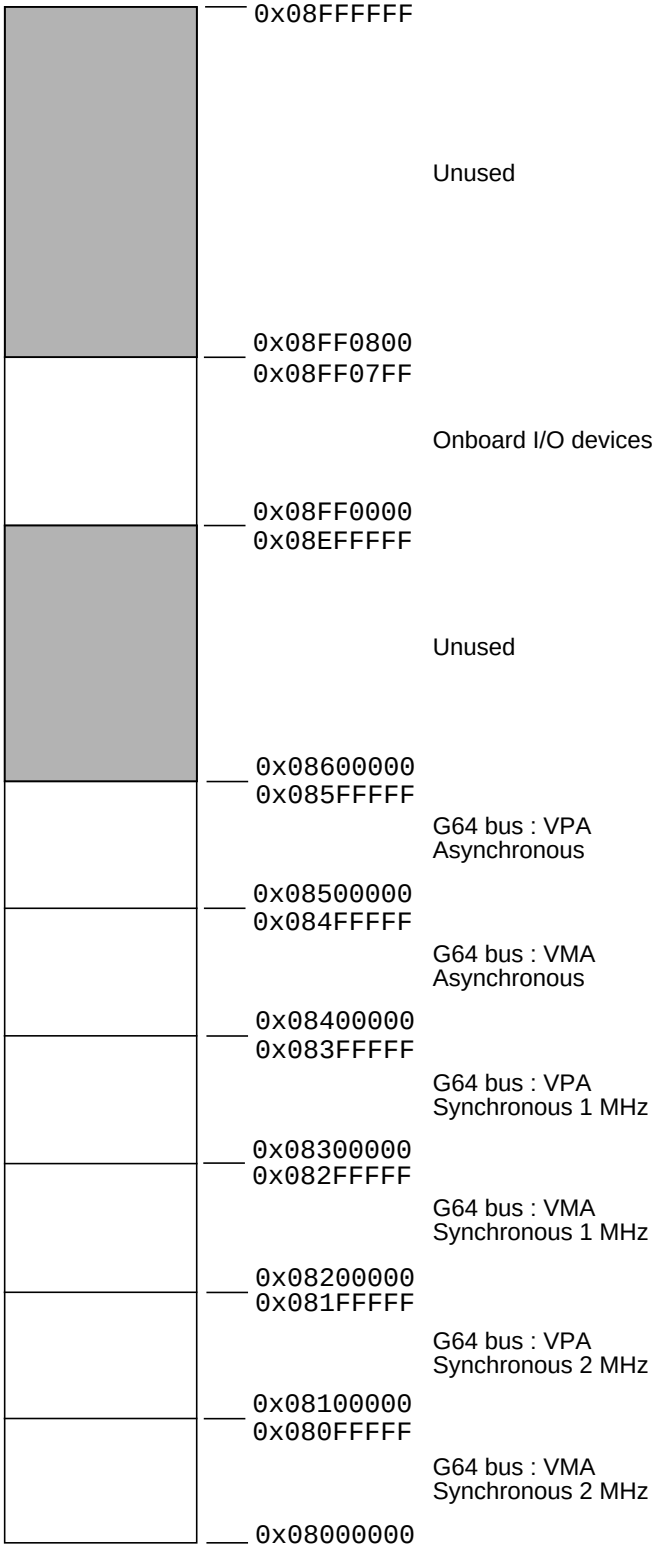


Figure 2. I/O Address Map

2.3 Onboard I/O Device Address Map

The onboard I/O device addresses are shown below.

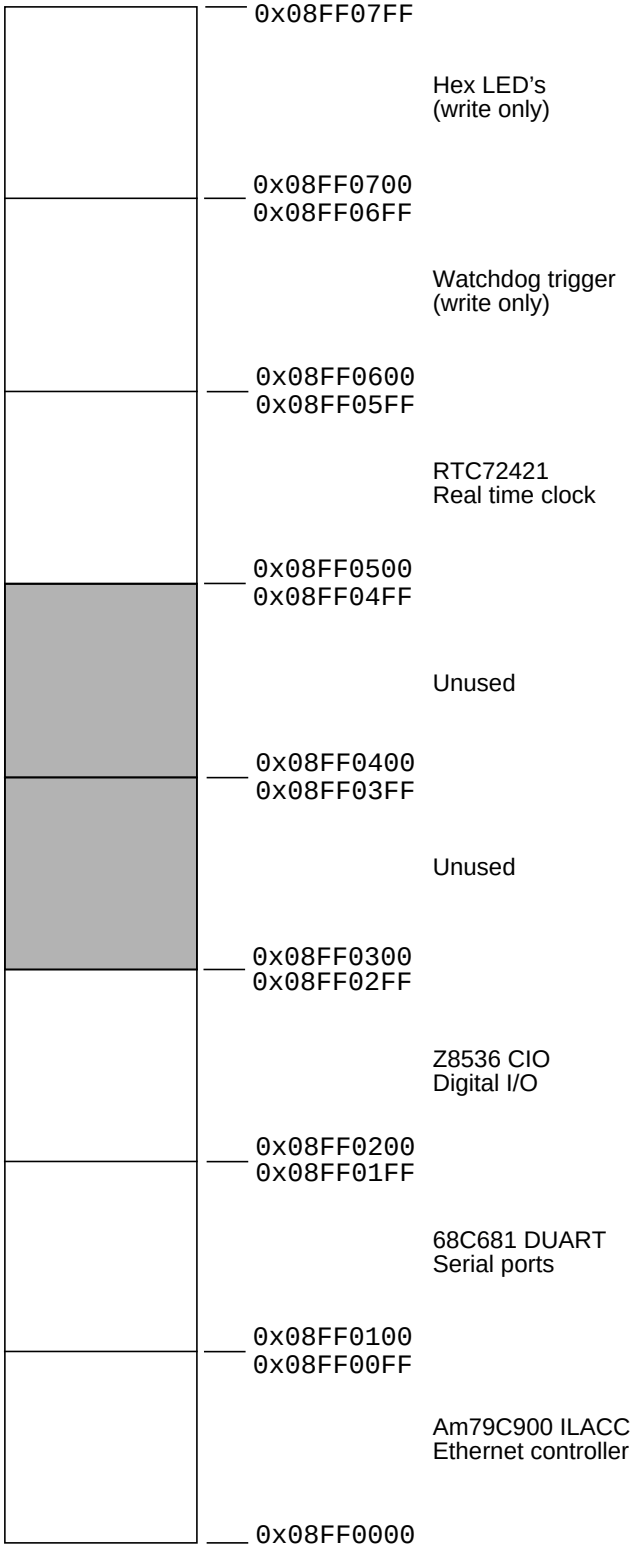


Figure 3. Onboard I/O Device Addresses

3. Configuration

3.1 Memory Device Type/Size : SW1, 2, 3

The type and size of the memory devices in each bank are set by means of three rotary hexadecimal coded switches, one for each bank. This allows the device size to be set as required simply by setting the switches instead of reconfiguring a large number of jumper links. The switches may be operated by using a small screwdriver or a trimmer adjustment tool.

The table below gives the device type and size for each switch setting.

Switch setting	Size	Type	Example part no.
0	32k×8	eprom	27C256
1	64k×8	eprom	27C512
2	128k×8	eprom	27C010
3	256k×8	eprom	27C020
4	512k×8	eprom	27C040
5-7	1M×8	eprom	27C080
8	32k×8	static ram	62256
9	64k×8	static ram	
A	128k×8	static ram	628128
B	256k×8	static ram	
C-E	512k×8	static ram	628512
F	Memory bank disabled		

Switch SW1 sets up memory bank 1, SW2 sets up bank 2, and SW3 sets up bank 3. They are located near the top left of the board, below the onboard battery and the MAX695 watchdog/reset controller.

If no devices are fitted to any memory bank, it must be disabled by setting its switch to position F. OS9 system errors occur if there is no memory fitted to an enabled memory bank.

3.2 Cache Disable : J1

Jumper J1 is used to disable the 68020 processor cache. If J1 is fitted, then the /CDIS cache disable input to the processor is held low, disabling the cache. If J1 is removed, /CDIS is pulled high, enabling the cache. For normal operation the cache is enabled, but in some situations, for example where a logic state analyser is used to trace bus cycles, it may be useful to disable the cache to allow all cycles to be traced.

3.3 Watchdog and Battery Configuration : J2

Jumper J2 is used to configure the watchdog and battery options.

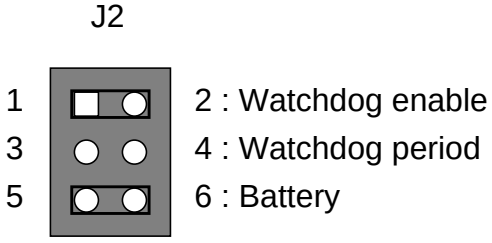


Figure 4. Watchdog and Battery Configuration : J2

Pins	Link	Function
1–2	in	enable watchdog
1–2	out	disable watchdog
3–4	in	watchdog period 100ms
3–4	out	watchdog period 1s
5–6	in	connect battery
5–6	out	disconnect battery

3.4 Interrupt Configuration : J3

Jumper J3 is used to connect the various interrupt sources to the interrupt priority encoder pal IC5.

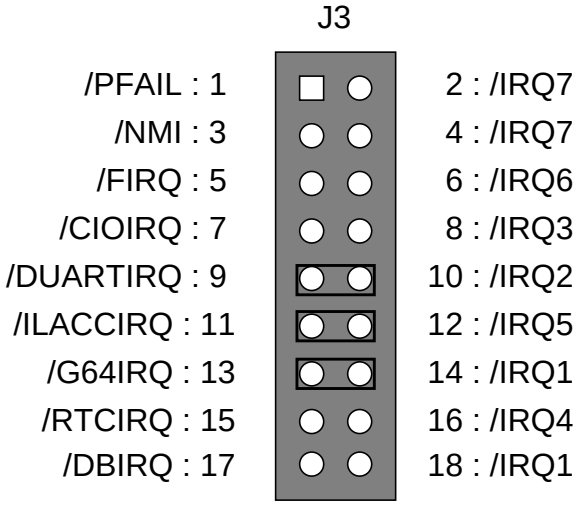


Figure 5. Interrupt Configuration : J3

The normal configuration is with the DUART interrupt connected to irq level 2, the ILACC interrupt connected to irq level 5, and the G64 bus /IRQ signal connected to irq level 1. The standard device descriptors supplied with the installed OS-9/68020 use these interrupt levels.

3.5 CIO Clock Frequency : J4

Jumper J4 sets the Z8536 CIO peripheral clock frequency as a power of 2 division of the main processor clock. The normal configuration is for a CIO clock of 6 MHz from a main processor clock of 12 MHz.

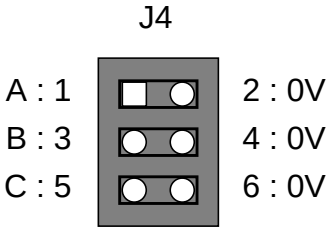


Figure 6. CIO Clock Frequency : J4

A link fitted connects the clock select line to 0V. The table below shows the clock division ratio for all link settings, and the peripheral clock speed for a 12 MHz main processor clock.

A	B	C	Clock Speed	Divisor
in	in	in	6 MHz	2
out	in	in	3 MHz	4
in	out	in	1.5 MHz	8
out	out	in	750 kHz	16
in	in	out	375 kHz	32
out	in	out	187.5 kHz	64
in	out	out	93.75 kHz	128
out	out	out	46.875 kHz	256

3.6 Memory Wait States : J5, J6, J9, J12

The numbers of wait states for each bank of memory are configured by jumpers J5, J6, J9 and J12.

J5	Boot eprom and eeprom (IC10 and IC11)
J6	Memory bank 1 (IC14–17)
J9	Memory bank 2 (IC21–24)
J12	Memory bank 3 (IC28–31)

Each wait state jumper is similar, with two links, and provides 0, 1, 2 or 3 wait states to the appropriate memory bank.

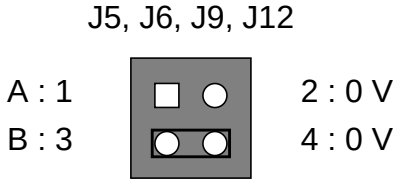


Figure 7. Memory Wait States : J5, J6, J9, J12

The table below shows the link settings for different numbers of wait states, with the maximum access times for each setting. These timings are for the standard configuration of a 16 MHz processor running with a 12 MHz clock, and 25 ns programmable logic devices.

Link 1–2	3–4	Wait States	Max. Access Time
out	out	0	100 ns
in	out	1	180 ns
out	in	2	260 ns
in	in	3	340 ns

NOTE : If the memory bank is configured for power-up write protection in battery backup applications (see jumpers J11, J13), then these maximum access times are reduced by 25 ns.

3.7 Memory Bank 1 Pin 1/VPP : J7

Jumper J7 allows pin 1 of the devices in memory bank 1 to be connected either to their normal pin 1 logic signal, for use with standard eproms or static rams, or to a VPP supply, for use with flash eproms up to a maximum device size of 512k×8.

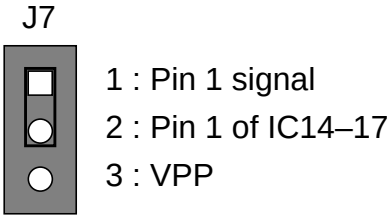


Figure 8. Memory Bank 1 Pin 1/VPP : J7

3.8 Memory Bank Pin 30/VCC : J8, J10, J14

Jumpers J8, J10 and J14 allow pin 30 of the devices in each memory bank to be connected either to their normal pin 30 logic signal, for use with 32 pin devices, or to the +5V power supply, for use with 28 pin devices (up to a maximum device size of 64k×8).

J8	Memory bank 1 (IC14–17)
J10	Memory bank 2 (IC21–24)
J14	Memory bank 3 (IC28–31)

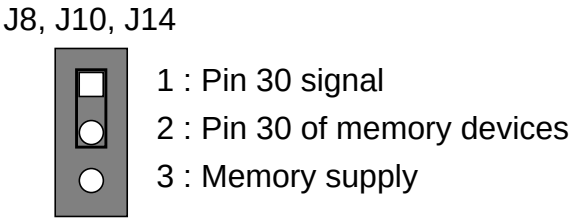


Figure 9. Memory Bank Pin 30/VCC : J8, J10, J14

3.9 Memory Banks 2 and 3 VCC/Battery Supply : J11, J13

Jumpers J11 and J13 allow memory banks 2 and 3 to be connected either to the normal +5V VCC supply, or to the +5V battery supply, for use in applications requiring battery-backed memory. They are also used to configure the /CE chip enable signals to the memory devices such that in battery backup applications, external protection circuits inhibit access to the memory devices until the power-up reset is complete, and the power supply is above 4.5V minimum. This guarantees that no spurious write signals can change data held in the battery-backed memories.

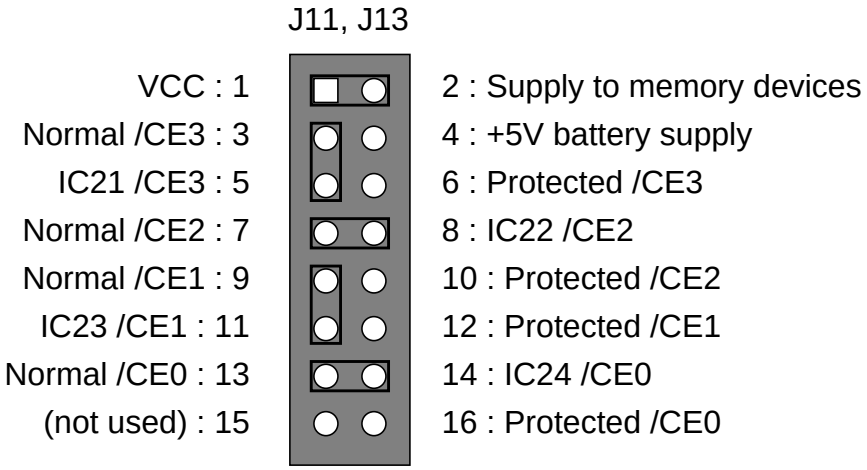


Figure 10. Normal Memory Configuration : J11, J13

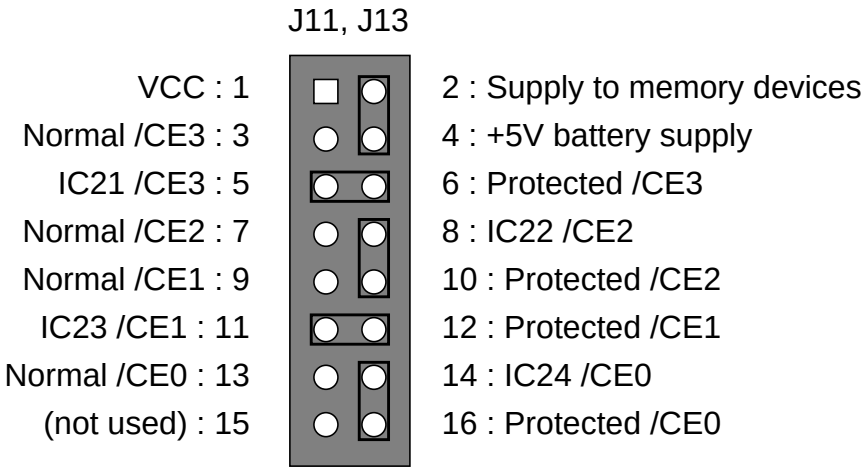


Figure 11. Battery Backup Memory Configuration : J11, J13

Jumper J11 sets up memory bank 2, and J13 sets up bank 3.

NOTE : If a memory bank is configured for power-up write protection as shown above, then the maximum access times for that bank are reduced by 25 ns. Please check the required number of wait states in this case.

3.10 G64 Bus Clock Speed : J15

Jumper J15 sets the basic speed of the E clock and SYSCLK signals for the G64 bus interface. If J15 is fitted, the E clock and SYSCLK signals are set to 1 MHz. If J15 is removed, the SYSCLK signal is a constant 2 MHz, and E clock is nominally 2 MHz, but allows stretched clock cycles for slower G64 bus modules where necessary. The default is for the G64 bus to be set for 2 MHz operation.

3.11 G64 Bus Configuration : J16, J17

Jumpers J16 and J17 are used to configure the G64 bus interface for either 8 bit or 16 bit data. J16 controls the logic signals for the bus interface, including the local processor /DSACKn signals, the G64 bus /DSn data strobes, and the enable signals for the G64 data bus transceivers. J17 is used to shift the processor address lines by one for use with the 16 bit data configuration, where the G64 bus uses word addresses, not byte addresses.

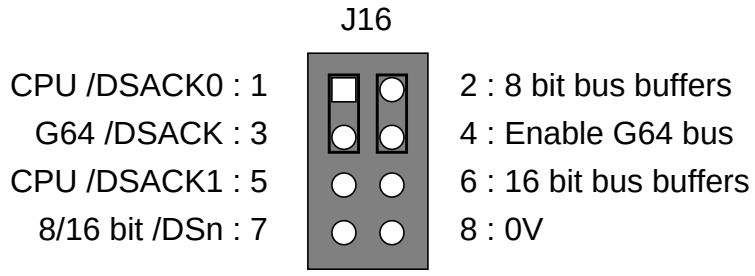


Figure 12. G64 Bus Control Signals (8 bit operation) : J16

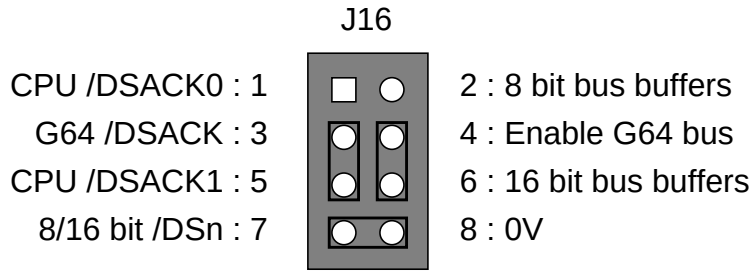


Figure 13. G64 Bus Control Signals (16 bit operation) : J16

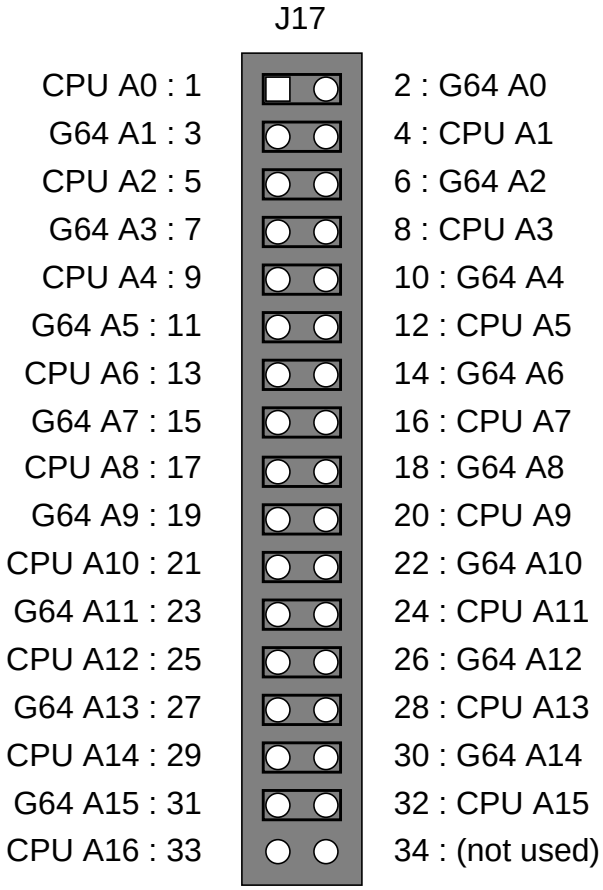


Figure 14. G64 Bus Address (8 bit operation) : J17

For 8 bit data operation, CPU address lines A15 to A0 are connected directly to the G64 bus address lines A15 to A0. The 8 bit data bus configuration uses G64 bus address lines A0 to A15 and A16 to A19, providing a 1M byte address space.

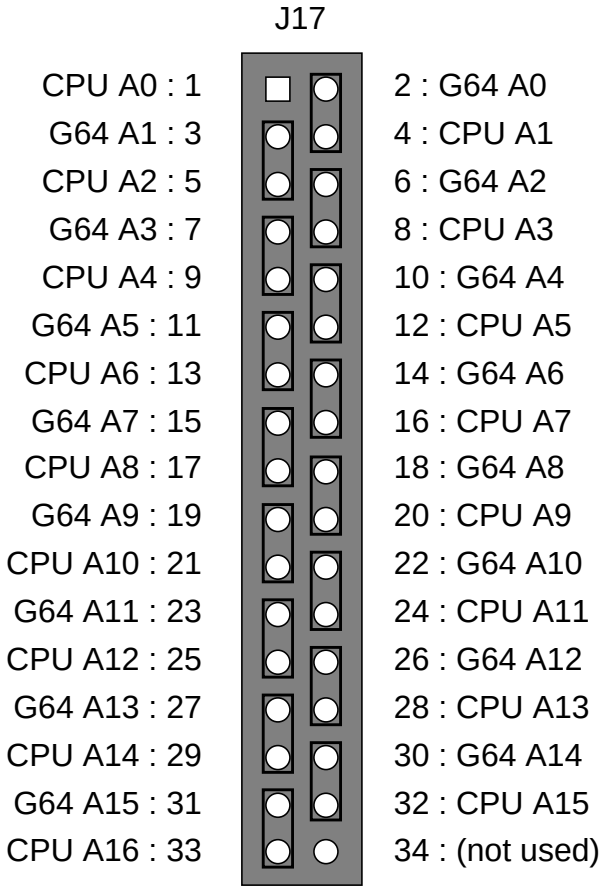


Figure 15. G64 Bus Address (16 bit operation) : J17

For 16 bit data operation, CPU address lines A16 to A1 are connected to the G64 bus address lines one lower, as the G64 address lines now represent a word address, not a byte address. The 16 bit data configuration uses G64 bus address lines A0 to A15, providing a 64k word address space.

3.12 Serial Eeprom Options : J18

Jumper J18 connects to pins 6 and 7 of the serial eeprom IC44. Normally this is a 93C46A type device, which does not use these pins. However, there are many different types of 8 pin serial eeprom devices, some of which now offer more advanced facilities such as programmable write protection of part of the stored data. J18 provides facilities for using some of these other devices which may require the use of pins 6 or 7 for enabling or disabling the new options. Typical examples of these options include device write protection, protection register enable, or parity enable features.

The two signals on pins 6 and 7 of the serial eeprom are also connected to inputs 3 and 4 on the 68C681 DUART device, to make the current state of J18 available to application software if required. Alternatively, if the serial eeprom does not make use of these pins, the jumper links may be used simply as configuration options, readable by startup software to configure an application for one of four possible setups.

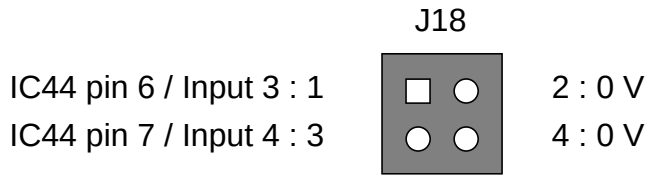


Figure 16. Serial Eeprom Options : J18

To set a line low, link it to 0V. To set a line high, leave the link off.

3.13 Serial Port Configuration : J19, J20, J21

The two serial ports on the CPU20 may be configured for various options. Each port may be configured independently of the other, using jumpers J19, J20 and J21.

J19 configures the three-state control for the RS-422/485 drivers. It allows the drivers to be permanently enabled, or to be enabled and disabled under control of the DUART device RTS output signal. It also allows the drivers to be permanently disabled, for use when the ports are configured for RS-232 operation.

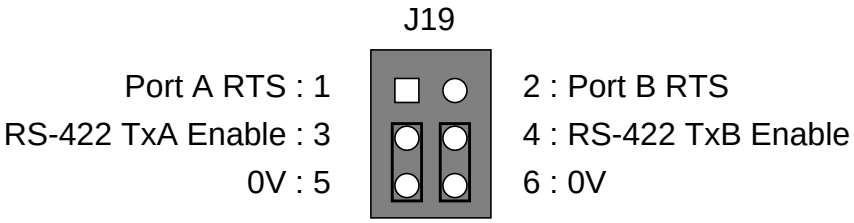


Figure 17. RS-422/485 Driver Enable : J19

Function	Port A Link	Port B Link
RS-422 disabled	3–5	4–6
RS-422 enabled	none	none
RTS control	1–3	2–4

J20 selects the RS-232 or RS-422/485 receivers for each port.

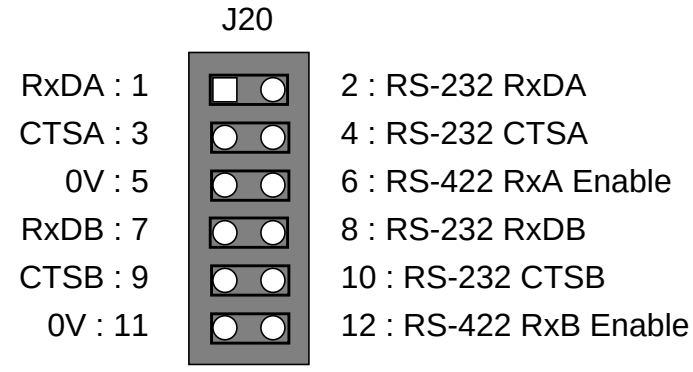


Figure 18. Serial Port Receiver Select : J20

Function	Port A Links	Port B Links
RS-232	1–2, 3–4, 5–6	7–8, 9–10, 11–12
RS-422/485	none	none

J21 enables the RS-232 drivers, and allows both the transmit/receive and RTS/CTS signal connections to be interchanged. Note that the RS-422/485 connections may not be interchanged.

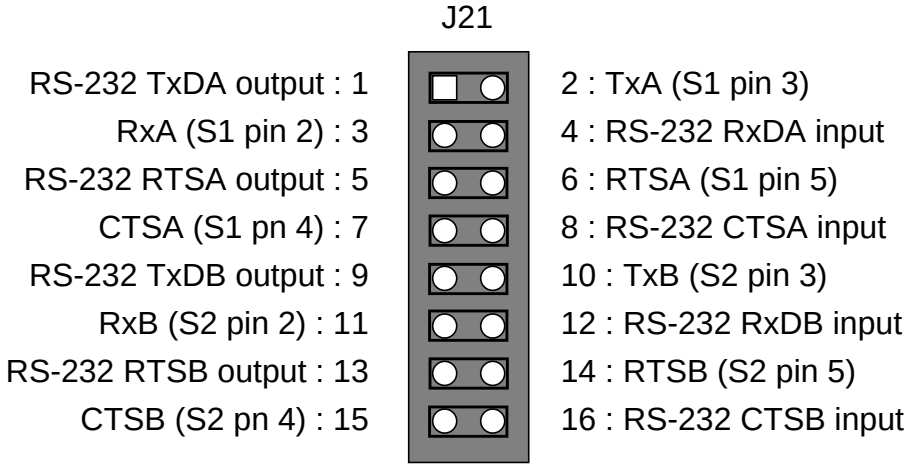


Figure 19. RS-232 Driver Enable and Port Connections : J21

Function	Port A Links	Port B Links
RS-232 normal	1–2, 3–4, 5–6, 7–8	9–10, 11–12, 13–14, 15–16
RS-232 reversed	1–3, 2–4, 5–7, 6–8	9–11, 10–12, 13–15, 14–16
RS-422/485	none	none

3.14 Ethernet Transceiver Enable : J22

Jumper J22 is used to enable the onboard Ethernet transceiver. If J22 is fitted, then the transceiver circuit is enabled. If J22 is removed, the transceiver is disabled.

3.15 Ethernet Heartbeat Signal : J23

Jumper J23 is used to enable or disable the collision detect heartbeat signal for the onboard Ethernet transceiver. If a link is fitted between pins 1 and 2, then the heartbeat signal is enabled. If a link is fitted between pins 2 and 3, the heartbeat signal is disabled. The heartbeat signal must be disabled for use with repeaters.

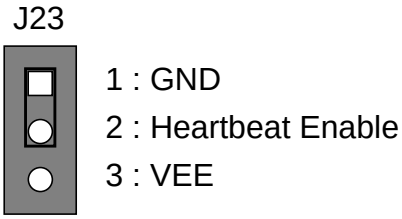


Figure 20. Ethernet Heartbeat Signal : J23

3.16 Memory Bank 3 Address : J24

Jumper J24 is used to select one of two possible arrangements for memory bank 3. For use as a completely separate third memory bank, it is configured at address 0x03000000 and is independent of bank 2. For use as an extension of memory bank 2, it is configured at an address contiguous with bank 2. In this case, bank 3 must be fitted with the same type and size of memories as bank 2, and the size/type selection switches SW2 and SW3 must be set to the same position.

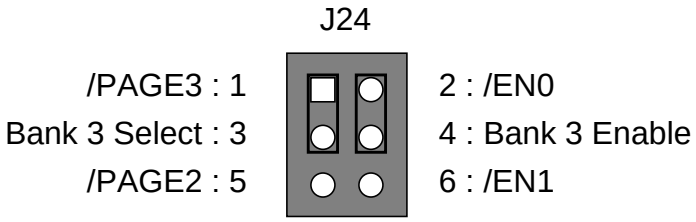


Figure 21. Memory bank 3 separately addressed : J24

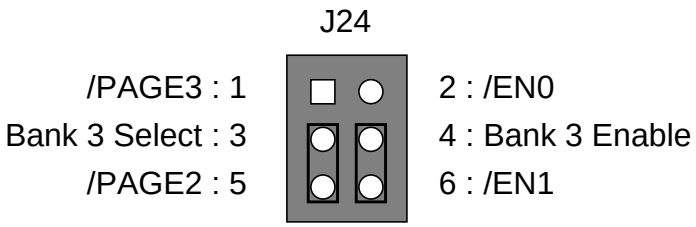
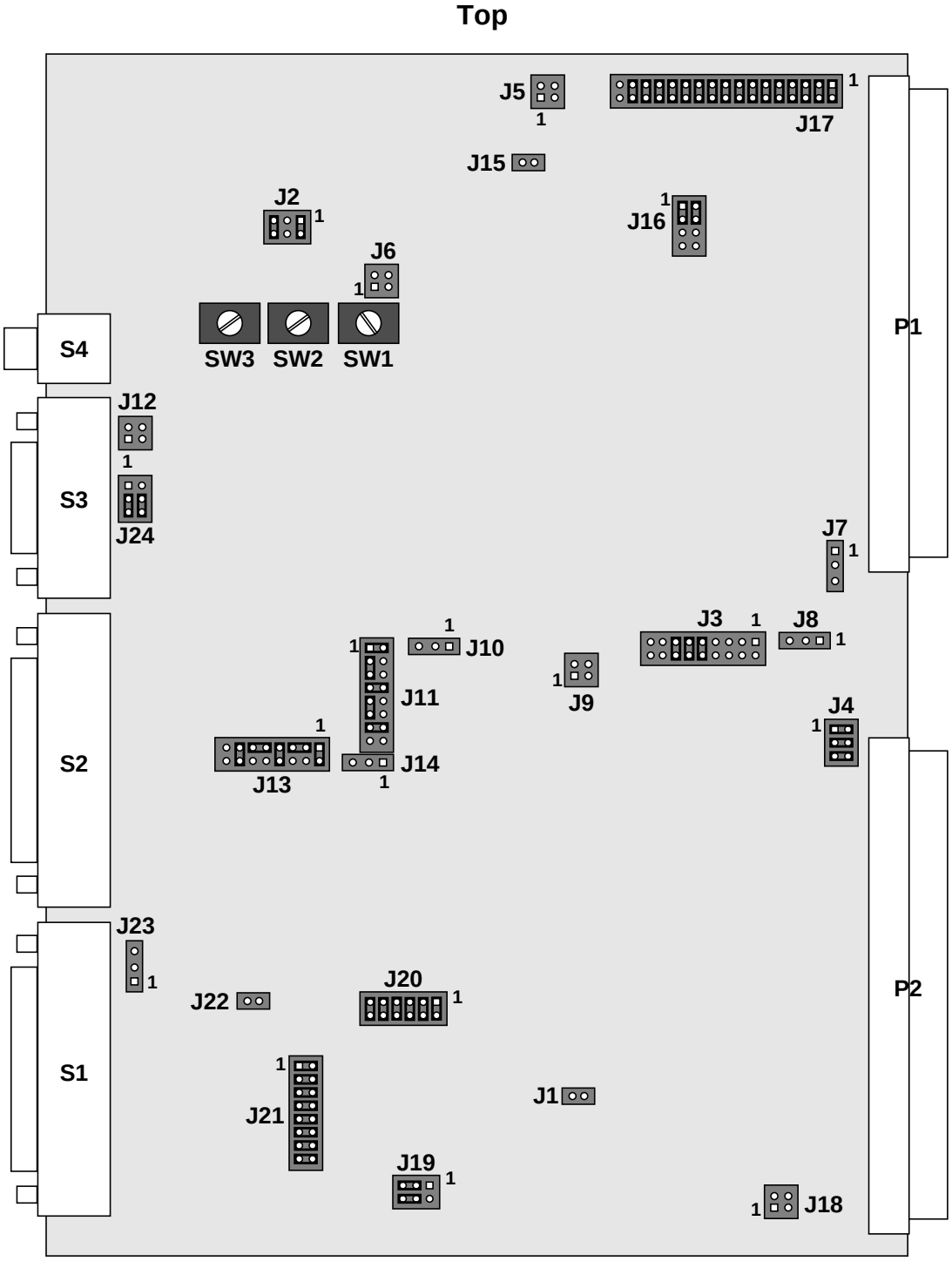


Figure 22. Memory bank 3 contiguous with bank 2 : J24

3.17 Switch and Jumper Locations



CPU20 module - component side

Figure 23. Switch and jumper locations

4. Connections

4.1 Signal Names

On all signals, a '/' prefix is used to denote an inverted or active low signal. For example, the /VPA signal is the active low Valid Peripheral Address signal on the G64 bus.

4.2 Power Supplies

The power supplies to the CPU20 module are connected via the 64 way G64 bus connector P1 and the general purpose I/O connector P2. The relevant pins are as follows:

0V	P1 pins 1a, 1b, 32a, 32b
	P2 pins 1a, 1c, 32a, 32c
+5V	P1 pins 31a, 31b
	P2 pins 2a, 2c, 31a, 31c
+12V	P1 pin 30a, P2 pin 30a
–12V	P1 pin 30b, P2 pin 30c
VPP	P1 pin 29a, P2 pin 29a
Vbatt	P1 pin 29b, P2 pin 29c

The CPU20 module requires only a single +5V supply for normal operation. If it is used with an external Ethernet transceiver, then a +12V supply is also required. The –12V connection is provided for use by any future daughter board expansion units. The VPP connection is provided for future support of Flash eprom devices in memory bank 1, although this facility is not currently supported. The Vbatt connection allows an external battery to be connected, for applications where the capacity of the onboard NiCad battery is not sufficient for the required data storage time.

4.3 Serial Port Connections : S1, S2

The pin functions for the serial port 25 way D sockets are shown below. The +5V supply is provided for use with the Quin PTS Operator's Panel.

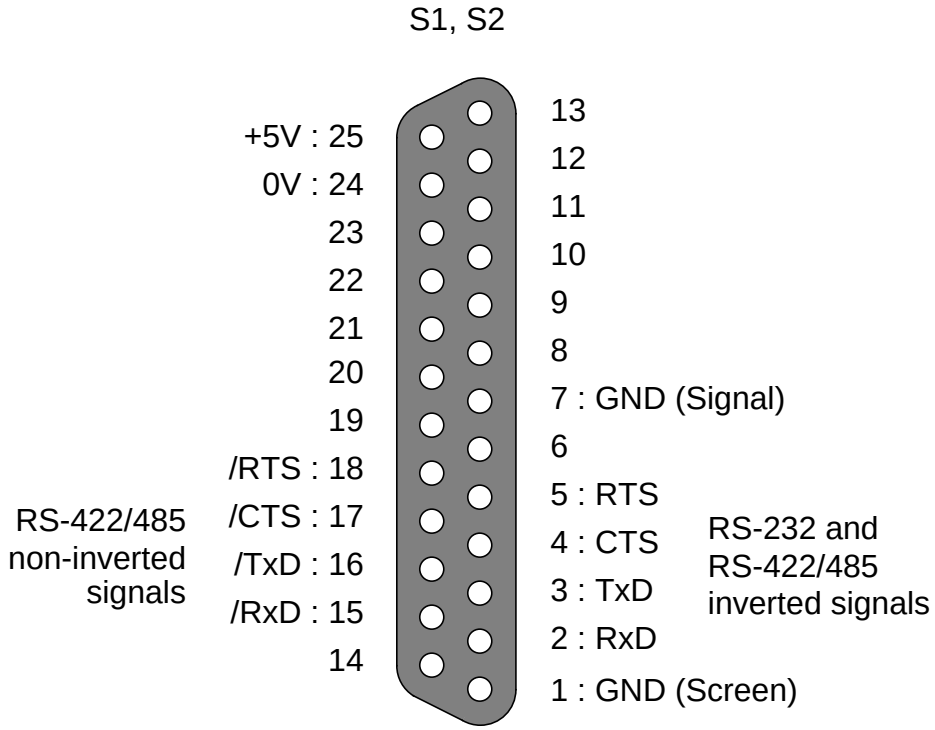


Figure 24. Serial Port Connections : S1, S2

4.4 Ethernet Drop Cable Connections : S3

The pin functions for the Ethernet 15 way D socket are shown below.

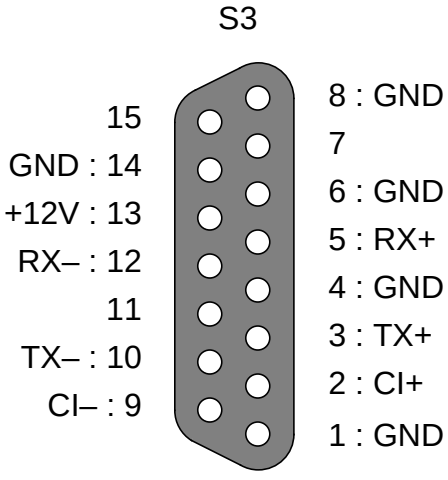


Figure 25. Ethernet Drop Cable Connections : S3

4.5 G64 Bus Connections : P1

The connections to the G64 bus (P1) are given in this table.

Signal	Pin number	Signal	Pin number
0V supply GND	1a	0V supply GND	1b
Address line A0	2a	Address line A8	2b
Address line A1	3a	Address line A9	3b
Address line A2	4a	Address line A10	4b
Address line A3	5a	Address line A11	5b
Address line A4	6a	Address line A12	6b
Address line A5	7a	Address line A13	7b
Address line A6	8a	Address line A14	8b
Address line A7	9a	Address line A15	9b
	10a		10b
Data strobe /DS0	11a	Data strobe /DS1	11b
	12a		12b
System clock SYSCLK	13a	E clock	13b
Valid peripheral address /VPA	14a	Reset /RESET	14b
Memory ready MRDY/DTACK	15a	Non-maskable interrupt /NMI	15b
Valid memory address /VMA	16a	Interrupt request /IRQ	16b
Read/write R/W	17a	Fast interrupt request /FIRQ	17b
	18a		18b
Address/data line A16/D8	19a	Data line /D12	19b
Address/data line A17/D9	20a	Data line /D13	20b
Address/data line A18/D10	21a	Data line /D14	21b
Address/data line A19/D11	22a	Data line /D15	22b
Data line /D0	23a	Data line /D4	23b
Data line /D1	24a	Data line /D5	24b
Data line /D2	25a	Data line /D6	25b
Data line /D3	26a	Data line /D7	26b
	27a		27b
	28a		28b
Flash memory VPP	29a	External battery Vbatt	29b
+12V supply	30a	–12V supply	30b
+5V supply VCC	31a	+5V supply VCC	31b
0V supply GND	32a	0V supply GND	32b

Figure 26. G64 Bus Connections : P1

4.6 General Purpose I/O Connections : P2

The general purpose input/output connections on plug P2 are given here.

Signal	Pin number	Signal	Pin number
0V supply GND	1a	0V supply GND	1c
+5V supply VCC	2a	+5V supply VCC	2c
Port line PA1	3a	Port line PA0	3c
Port line PA3	4a	Port line PA2	4c
Port line PA5	5a	Port line PA4	5c
Port line PA7	6a	Port line PA6	6c
Port line PC1	7a	Port line PC0	7c
Port line PC3	8a	Port line PC2	8c
0V	9a	0V	9c
Port line PB1	10a	Port line PB0	10c
Port line PB3	11a	Port line PB2	11c
Port line PB5	12a	Port line PB4	12c
Port line PB7	13a	Port line PB6	13c
Port line PC1	14a	Port line PC0	14c
Port line PC3	15a	Port line PC2	15c
0V	16a	0V	16c
	17a		17c
	18a		18c
	19a		19c
	20a		20c
	21a		21c
	22a		22c
	23a		23c
	24a		24c
	25a		25c
	26a		26c
	27a		27c
	28a		28c
Flash memory VPP	29a	External battery Vbatt	29c
+12V supply	30a	–12V supply	30c
+5V supply VCC	31a	+5V supply VCC	31c
0V supply GND	32a	0V supply GND	32c

Figure 27. General Purpose I/O Connections : P2

4.7 Daughter Board Expansion : S5, S6

The daughter board expansion connections are given below.

Signal	Pin number	Signal	Pin number	Signal	Pin number
A21	1a	A22	1b	A23	1c
A18	2a	A19	2b	A20	2c
A15	3a	A16	3b	A17	3c
A12	4a	A13	4b	A14	4c
A9	5a	A10	5b	A11	5c
A6	6a	A7	6b	A8	6c
A3	7a	A4	7b	A5	7c
A0	8a	A1	8b	A2	8c
FC0	9a	FC1	9b	FC2	9c
/PAGE1	10a	/PAGE2	10b	/PAGE3	10c
/PAGE4-7	11a	/SPARE1	11b	/SPARE2	11c
/BR	12a	/BG	12b	/BGACK	12c
/RD	13a	/WR	13b	/IOPAGE	13c
/DBIRQ	14a	–12V	14b	+12V	14c
+5Vbatt	15a	VPP	15b	+5V	15c
CLK	16a	/CLK	16b	0V	16c

Figure 28. Daughter Board Expansion Connector : S5

Signal	Pin number	Signal	Pin number	Signal	Pin number
D30	1a	D31	1b	/RESET	1c
D28	2a	D29	2b	/AS	2c
D26	3a	D27	3b	/DS	3c
D24	4a	D25	4b	R/W	4c
D22	5a	D23	5b	SIZ1	5c
D20	6a	D21	6b	SIZ0	6c
D18	7a	D19	7b	/DSACK1	7c
D16	8a	D17	8b	/DSACK0	8c
D14	9a	D15	9b	/DT32	9c
D12	10a	D13	10b	/DT16	10c
D10	11a	D11	11b	/DT8	11c
D8	12a	D9	12b	/WT1	12c
D6	13a	D7	13b	/WT0	13c
D4	14a	D5	14b	/RamEnable	14c
D2	15a	D3	15b	+5V	15c
D0	16a	D1	16b	0V	16c

Figure 29. Daughter Board Expansion Connector : S6

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