Quin Systems Limited

CPU360 Issue D Hardware Manual

Issue 3

December 1997

(MAN530)

Copyright Notice

Hardware Issue

This manual reflects the Issue D CPU360 hardware.

Important Notice

Quin Systems reserves the right to make changes in the products described in this document in order to improve design or performance and for further product development. Examples given are for illustration only, and no responsibility is assumed for their suitability in particular applications. Reproduction of any part hereof without the prior written consent of Quin Systems is prohibited.

Although every attempt has been made to ensure the accuracy of the information in this document, Quin Systems assumes no liability for inadvertent errors.

Suggestions for improvements in either the products or the documentation are welcome.

Contents

List of Figures

1. Introduction

This document describes the Quin Systems CPU360 single board computer.

The CPU360 module is a medium performance 32-bit processor module, based around the Motorola 68EN360 integrated processor. It is designed specifically for standalone operation in rom-based embedded systems, and in particular is used in the PTS range of systems. It offers eprom, dram and non-volatile memory, various serial ports, an Ethernet port with AUI and twisted pair interfaces, and two CANbus interfaces. It also has provision for an optional 68040 processor if more performance is required.

The CPU360 provides four 32-pin JEDEC sockets for eproms or flash roms, allowing a maximum of 4 Mbytes using 1M×8 devices. It normally has 1 Mbyte of dram, configured as 256k×32 in two devices, 128k bytes of eeprom, and 128k bytes of battery backed sram. These are used for non-volatile data storage. It also has a small serial eeprom device which is used to store the Ethernet physical address and any software license keys.

Four serial ports are available on the 68EN360 processor. One is dedicated to the Ethernet port, one is reserved for use with a protocol-specific daughter board, and the remaining two are configurable separately for RS-232 or RS-485 operation. A Z8536 device provides up to 20 digital input/output lines at LSTTL levels, and up to three counter/timers. A calendar/clock device with battery backup provides date/time information. A hardware watchdog timer is also available.

The Ethernet interface provides access to local area networks. It may be used with the onboard 10 base T twisted pair transceiver, or via the AUI port with an external transceiver for connection to other media such as thick or thin coax.

The two CANbus interfaces are compatible with the CAN in Automation (CiA) draft standard DS102 Version 2.0, CAN Physical Layer for Industrial Applications. They are electrically isolated and fully independent. Each has both a plug and a socket connected in parallel to allow for simple cable connection between units.

The board supports a range of daughter board communications modules made by Hilscher GmbH. These offer a range of communications protocols and interfaces, including Profibus and Interbus-S.

Offboard expansion is available via the G64 bus, which supports a wide range of third party input/output modules. It has a 16 bit data bus and a 16 bit address bus, and supports both synchronous and asynchronous bus cycles.

2. Using the CPU360

2.1 Processor Selection

The 68360 processor config pins select the initial bus size, and whether it is in normal cpu or slave mode. For normal use with the cpu32+ processor core enabled, 32 bit rom chip select, set config210 to 100 by fitting links to jumper J7 pins 1-2 and 3-4. Also link J7 pins 7-8 so that all devices return DSACKn for 32 bit transfers. For use with the 68040 in companion mode, config210 should be set to 011 by removing links from J7 pins 1-2 and 3-4, and linking J7 pins 5-6. Also remove the link from J7 pins 7-8 as the 68040 only uses a single DSACK signal, and all transfers are 32 bits wide.

2.2 Software Control

The CPU360 board makes extensive use of the programmable features of the 68360 cpu and its system integration module (SIM). These must be correctly set up by any application or system software when the board starts up. A brief description of the various control lines used by the CPU360 is given in the following sections.

2.3 Chip Selects

The programmable chip select pins are used as follows :

CS0	eprom, 256k×32, 512k×32, or 1M×32
CS1	dram /RAS, 256k×32
CS2	sram, 128k×8, battery backed
CS3	eeprom, 128k×8
CS4	I/O devices (RTC, CAN, CIO)
CS5	G64 bus

Only the CS0 chip select is active when the processor starts after a hard reset. All other chip select address ranges and options must be set by the boot software. Note that the sram and eeprom devices are 8 bits wide, but are accessed on the 32 bit processor bus to allow for the optional 68040 cpu. This means that they can only be accessed on every 4th byte.

Because the CPU360 module uses the programmable chip select outputs for the rom, ram and i/o areas, the address map is determined by the software at startup. A suggested address map is shown in the following table.

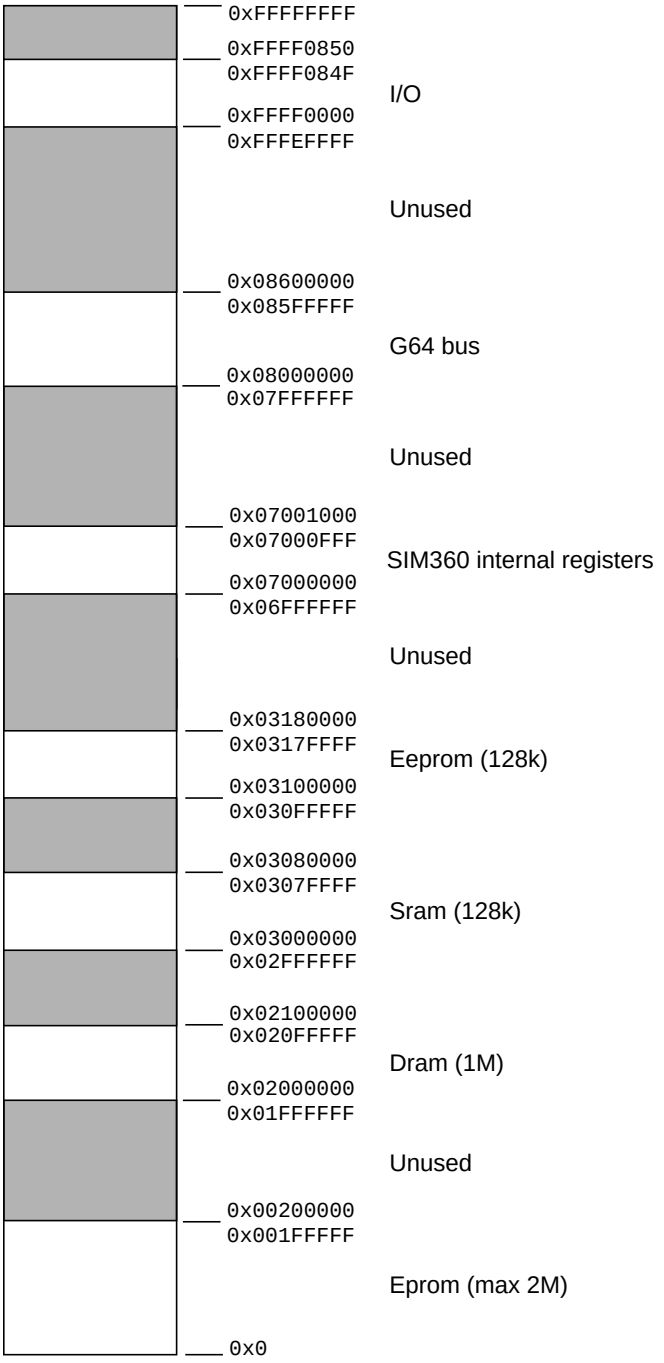


Figure 1. Address map

2.4 G64 Bus Address Map

The address map within the G64 bus address space is shown below. Note that the G64 data bus is 16 bits wide, but is accessed on the 32 bit processor bus to allow for the optional 68040 cpu. This means that G64 bus locations are accessed on alternate words.

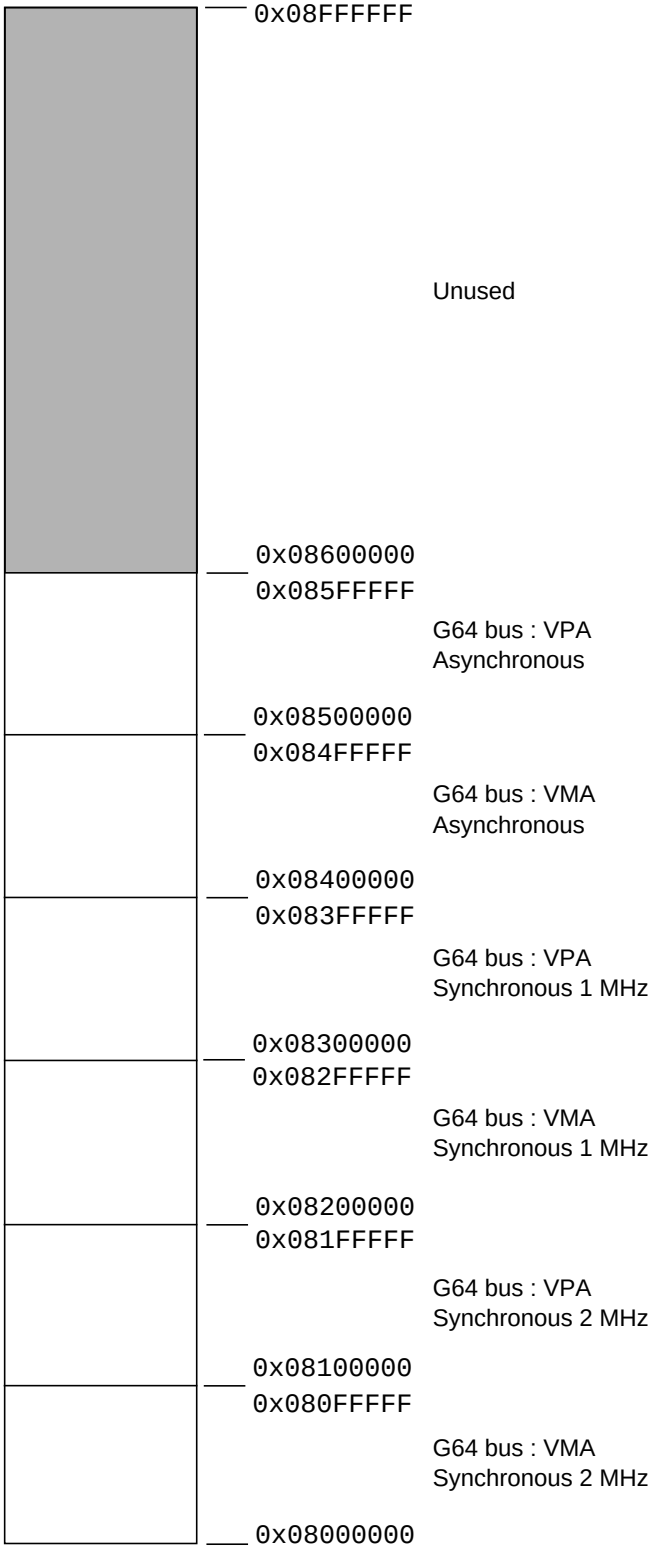


Figure 2. G64 bus address map

2.5 I/O Address Map

The address map for the CPU360 I/O devices is shown below. Note that these devices are all 8 bits wide, but are accessed on the 32 bit processor bus to allow for the optional 68040 cpu. This means that the device registers are accessed on every 4th byte only.

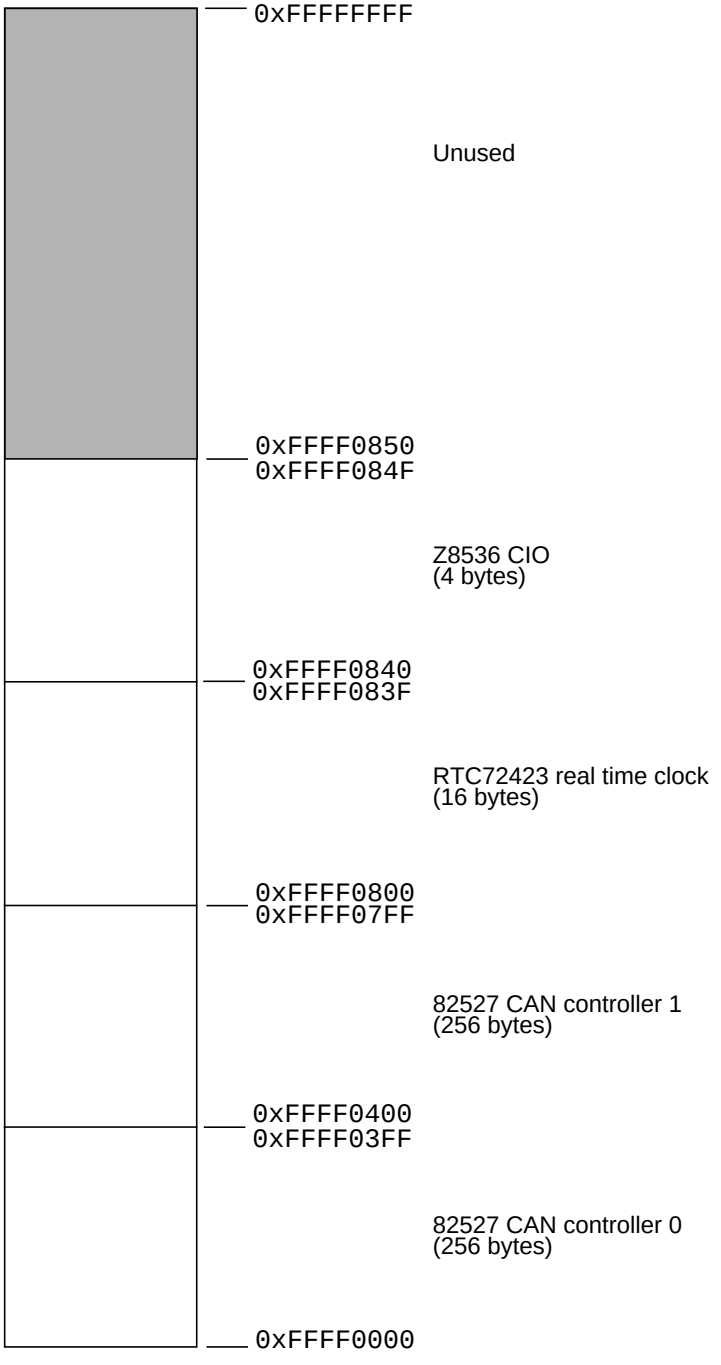


Figure 3. I/O address map

2.6 68360 Internal Registers

In the 68360 processor, the internal registers in the SIM module and the dual port ram for the communications processor module (CPM) occupy an 8k byte block. This block is located on any 8k byte boundary by programming the module base address register MBAR. The standard software in the PTS systems locates the internal memory at address 0x07000000.

The MBAR is located at address 0x0003FF00 in cpu space. Note that this does not conflict with the CS0 chip select address range, as any cpu space access to any global internal registers does not assert external chip select pins. Accessing the MBAR requires the use of the MOVES instruction with the SFC or DFC source/destination function code registers containing the function code for cpu space. Please refer to page 6-3 in the 68360 User's Manual for more details.

2.7 Memory Control Signals

The port E pins need to be programmed for use with the memory configuration used on the CPU360 board by programming the port E pin assignment register PEPAR. Set bit 7 to 1 to enable /WE0-3 instead of A28-31. Set bit 6 to 1 to enable the AMUX function for dram address multiplexer control. Set bits 4 and 2 to 0 to select the /CAS0-3 functions for the dram column address strobes. For more details on setting up the memory controller and chip select pins, please refer to the 68360 User's Manual, chapter 6.

2.8 Memory Sizes

The CPU360 issue D supports the following memory sizes.

EPROM	256k×32, 512k×32, or 1M×32	(four devices)
DRAM	256k×32 or 1M×32	(factory fitted only)
SRAM	128k×8 or 512k×8	(factory fitted only)
EEPROM	128k×8, 256k×8, or 512k×8.	

Note that the larger size dram and sram options must be specified when the CPU360 board is ordered, as they are surface mount packages and are soldered directly to the board.

Also note that the use of larger memory devices may require software changes to correctly set up the programmable chip select pins on the 68360 processor.

2.9 Communications Ports

The serial communications ports on the CPU360 are very flexible, and use the CPM communications processor module on the 68EN360 cpu. The four ports are allocated as follows to the four serial communications controllers (SCCs) on the 68EN360.

SCC1	Ethernet
SCC2	Daughter board (for example, isolated RS-485 for Bitbus)
SCC3	Serial port B
SCC4	Serial port A

The 68EN360 cpu has some software control over various functions of each port, usually by means of programmable output port pins.

2.10 Ethernet Port

The Ethernet port uses all of the signal lines available to SCC1.

PA0	RXD1
PA1	TXD1
PC0	TENA
PC4	CLSN
PC5	RENA
PA8	TCLK1
PA9	RCLK1

The Ethernet transceiver device, the 68160, has several programmable functions. These are controlled by output lines on port B. Refer to the 68160 data sheet for more details.

PB10	Twisted pair enable
PB11	Twisted pair auto polarity check
PB12	/Twisted pair full duplex
PB13	/Twisted pair heartbeat
PB14	Auto twisted pair detect
PB15	Loopback
PB16	Standby

2.11 Daughter Board Port

Serial channel SCC2 is connected to daughter board socket XS6. It uses the following port pins.

PA2	RXD2
PA3	TXD2
PC1	RTS2
PC6	CTS2
PC7	CD2
PA10	TCLK2
PA11	RCLK2
PB4	MODE0
PB5	MODE1

The function of these pins depends on the particular hadrware present on the daughter board. Standard daughter boards will be made available for specific communications interfaces as required. For example, a Bitbus interface board provides an isolated RS-485 interface with software control using the mode signals to select between synchronous or self-clocked modes, and the data rate for self-clocked operation. The daughter board uses XS3 and/or XS5 to bring its external signals out to two D type sockets on the CPU360.

2.12 Serial Ports

The two standard serial ports use programmable RS-232/485 transceivers. These are controlled by output port signals from the processor, and need to be set up appropriately by the system software.

Port B uses the following pins.

PA4	RXD3
PA5	TXD3
PC2	RTS3
PC8	CTS3
PC9	CD3

Port A uses the following pins.

PA6	RXD4
PA7	TXD4
PC3	RTS4
PC10	CTS4
PC11	CD4

Each port may be set up for RS-232, RS-485 point-to-point (enabled), or RS-485 multidrop with tristate control. When RS-232 mode is selected, ports A and B support hardware handshake using the RTS/CTS signals, and an optional CD carrier detect signal for use with modems.

Port B (SCC3)

Mode PB8	PC2
RS-2320	RTS3
RS-4851	tristate control (0=enabled, 1=disabled)

Port A (SCC4)

Mode PB9	PC3
RS-2320	RTS4
RS-4851	tristate control (0=enabled, 1=disabled)

Port A also has a jumper to allow it to be forced into RS-232 mode if required. Normally a link is fitted to J9 pins 1–2 for software control as described above. If this link is removed, then port A is set to RS-485 mode. If the link is fitted to J9 pins 2–3, then RS-232 mode is selected.

2.13 Serial Eeprom

The following port pins are used for the serial eeprom device. This is normally an SPI compatible device, a Xicor X25040, having a capacity of 4k bits (512×8).

PB0	/SPISEL serial eeprom enable
PB1	SPICLK serial eeprom clock
PB2	SPIMOSI data output to serial eeprom
PB3	SPIMISO data input from serial eeprom

2.14 Other Signals

Other port lines are used as follows.

PA12	Green LED (low = on)
PA13	Red LED (low = on)
PA14	Hardware watchdog trigger
PA15	Hardware watchdog status (low = watchdog tripped)

2.15 CANbus Ports

The CPU360 module supports two separate CANbus ports. These use the Intel 82527 CANbus controller, which supports both CAN 1 and CAN 2 protocols. The hardware implementation of the physical layer is fully isolated and uses the Philips 82C250 transceiver which operates at a bit rate of up to 1Mbit/second. It complies with the CAN in Automation (CiA) draft standard DS102 Version 2.0, CAN Physical Layer for Industrial Applications.

The CANbus implementation requires an external power supply to provide power to the isolated transceivers. If the CANbus is disconnected, or the power supply is not present, then the CANbus interface will not operate. An optocoupler device is connected to the CANbus network power supply, and allows software to detect whether or not it is present.

2.16 Daughter Board

The CPU360 board supports a range of standard communications modules made by Hilscher GmbH. These offer several different protocols and interfaces, including Profibus and Interbus-S. The modules connect to the CPU360 board via daughter board connector XP1. XS2 and XS4 connect status and error signals to the front panel LED indicators. The communications link signals use XS5 to connect to one of the 9 way D sockets on the CPU360. The high speed communications modules use a local processor with a dual port memory interface to the CPU360. These use a local serial port to configure the communications module, which is via XS3 to the second 9 way D socket.

3. Configuration

3.1 Eprom/Flash Pin 31 : J1

J1 selects the signal connected to pin 31 of the eprom or flash rom devices in sockets IC3-6. For 27C020 or similar eproms (256k×8), link pins 1 and 2 only. For 27C040 eproms (512k×8) or larger, link pins 1–2 and 3–4. For all flash roms, no links should be fitted to J1.

3.2 Eprom/Flash Pin 1 : J2

J2 selects the signal connected to pin 1 of the eprom or flash rom devices in sockets IC3-6. For most eproms and flash devices, no link should be fitted to J2. For 27C080 eproms (1M×8), link pins 1 and 2. For 29F040 flash roms, link pins 2 and 3.

3.3 Dram Burst Addressing : J3

Jumper J3 allows the dram memory to be configured for burst cycles when used with the optional 68040 processor. For normal operation with the 68360 processor, link pins 1–3 and 2–4. To allow burst cycle operation with the optional 68040 processor, link pins 3–5 and 4–6.

3.4 Serial Eeprom Write Protect : J4

To write protect the serial eeprom device IC16, fit a link to jumper J4.

3.5 Interrupt Configuration : J5

Jumper J5 is used to connect various interrupt sources to the seven processor interrupt inputs.

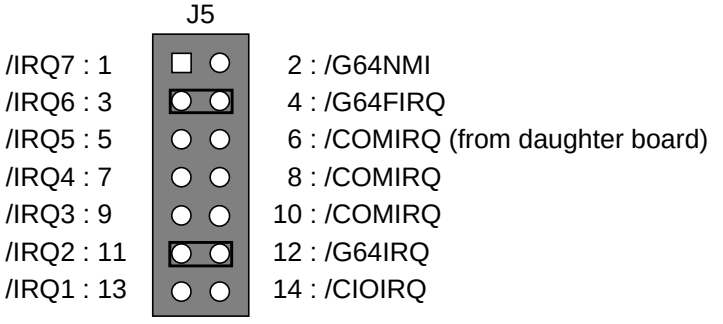


Figure 4. Interrupt configuration : J5

The normal configuration is with the G64 bus /FIRQ interrupt connected to level 6, and the G64 bus /IRQ signal connected to irq level 2. The standard firmware supplied with the PTS system uses these interrupt levels.

3.6 Reset and Watchdog : J6

Jumper J6 sets up options for the hardware watchdog and reset device. Link pins 1 and 2 to give a manual reset signal to the processor. Link pins 3 and 4 to enable the external hardware watchdog. Link pins 5 and 6 to enable the external hardware reset to the processor. Pins 7 and 8 connect the rechargeable battery to the VBB supply rail for the battery backed memory and real time calendar/clock devices. The normal configuration is with links fitted to pins 5–6 and 7–8.

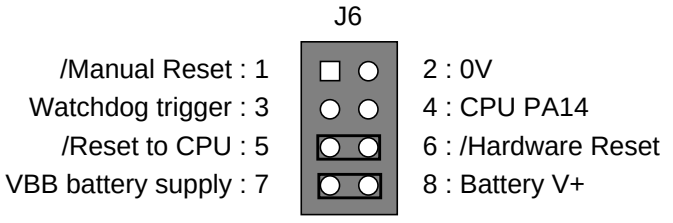


Figure 5. Reset and watchdog : J6

3.7 Processor Configuration : J7

Jumper J7 is used to set the processor configuration. For normal use with the 68360 cpu, link J7 pins 1–2, 3–4 and 7–8. For use with the optional 68040 cpu, link J7 pins 5–6 only. To disable the MMU on a full 68040 cpu, link J7 pins 11 and 12. This has no effect on the 68360 cpu, or on other variants of the 68040 such as the 68EC040 or 68LC040.

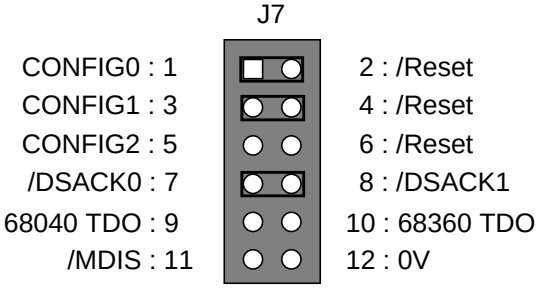


Figure 6. Processor configuration : J7

3.8 CIO Clock Frequency : J8

Jumper J8 sets the Z8536 CIO peripheral clock frequency as a power of 2 division of the main processor clock. The normal configuration is for a CIO clock of 6 MHz from a main processor clock of 24 MHz.

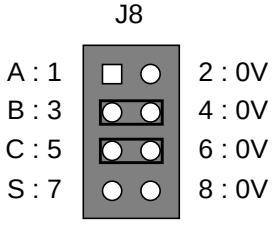


Figure 7. CIO clock frequency : J8

A link fitted connects the clock select line to 0V. The table below shows the clock division ratios for all link settings, and the peripheral clock speeds for a 24 MHz main processor clock.

A	B	C	Divisor	24 MHz
in	in	in	2	12 MHz
out	in	in	4	**6 MHz** (default)
in	out	in	8	3 MHz
out	out	in	16	1.5 MHz
in	in	out	32	750 kHz
out	in	out	64	375 kHz
in	out	out	128	187.5 kHz
out	out	out	256	93.75 kHz

The clock oscillator enable input (pin S) is also brought to J8. This is to allow the clock to be disabled during board testing, and is not used in normal operation..

3.9 Serial Port A Override : J9

The serial ports on the CPU360 module are configured by the software for RS-232 or RS-485 as required, to reduce the number of jumpers that need to be configured by the customer for different applications. Jumper J9 allows the software configuration for port A to be overridden for testing. For normal operation under software control, link J9 pins 1 and 2. To force RS-232 operation, link pins 2 and 3. To force RS-485 operation, remove the link.

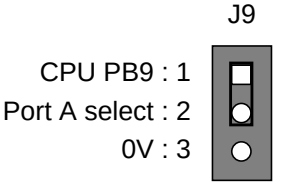


Figure 8. Serial port A override : J9

3.10 Static Ram Size : J10

The CPU360 module can support a 128k×8 or a 512k×8 static ram device. Jumper J10 sets the appropriate address line configuration. For normal operation with a 128k×8 device (e.g. HM628128), link J10 pins 1 and 2. For use with a 512k×8 device (e.g. HM628512), link pins 2 and 3. Note that the larger static ram is only available if specified when the CPU360 is ordered, as the device is in a surface mount package and is soldered directly to the circuit board.

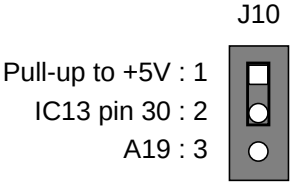


Figure 9. Static ram size : J10

3.11 CANbus Interrupts : J11

Jumper J11 is used to set up the interrupt signals from the two CANbus interfaces. Note that the two interfaces may use the same interrupt or two different processor interrupts if required.

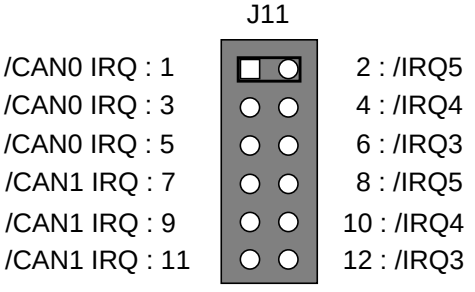
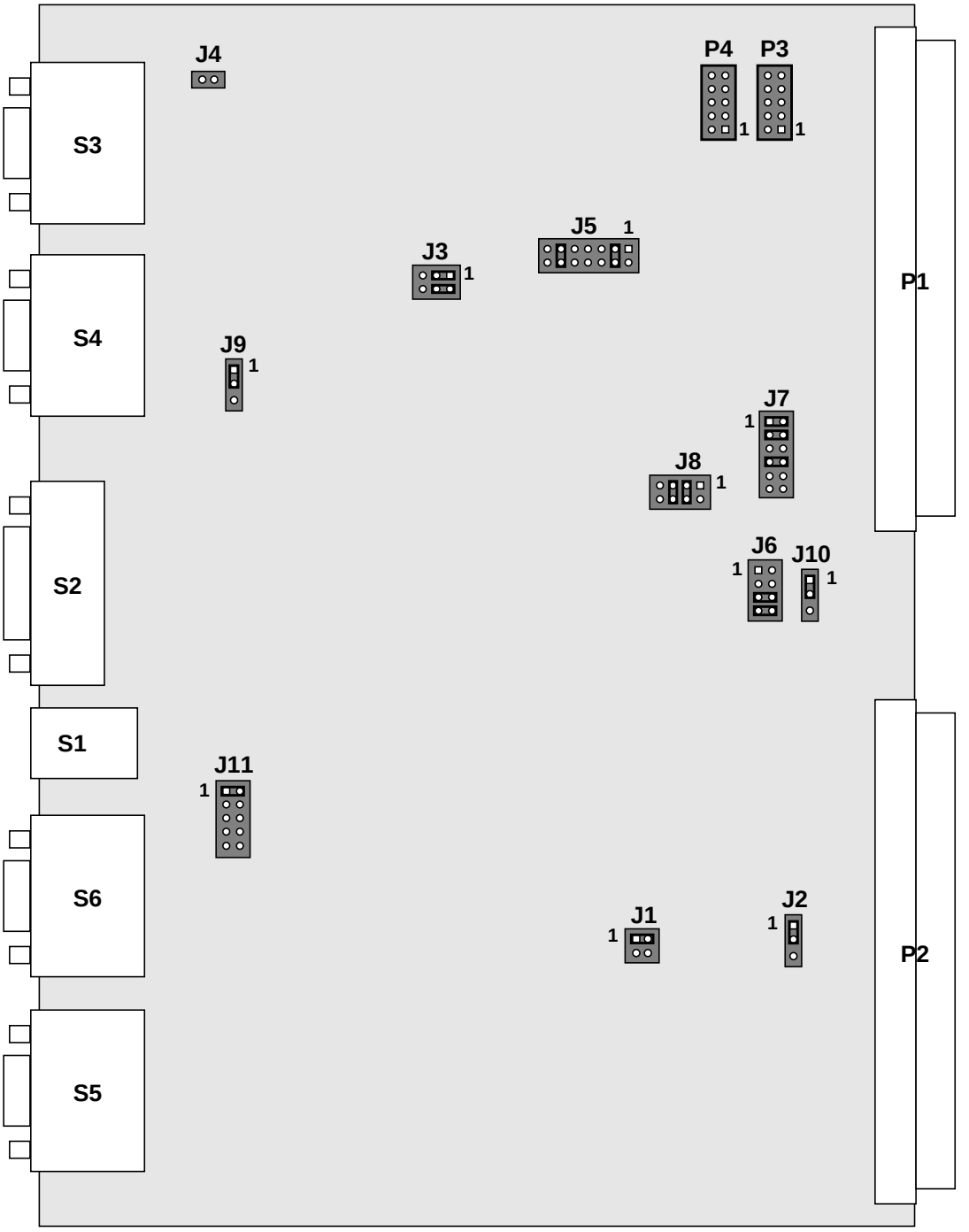


Figure 10. CANbus interrupts : J11

3.12 Jumper Locations

CPU360 module - component side

Top



Bottom

Figure 11. Jumper locations

4. Connections

4.1 Signal Names

On all signals, a '/' prefix is used to denote an inverted or active low signal. For example, the /VPA signal is the active low Valid Peripheral Address signal on the G64 bus.

4.2 Power Supplies

The power supplies to the CPU360 module are connected via the 64 way G64 bus connector P1 and the general purpose I/O connector P2. The relevant pins are as follows:

0V	P1 pins 1a, 1b, 32a, 32b
	P2 pins 1a, 1c, 32a, 32c
+5V	P1 pins 31a, 31b
	P2 pins 2a, 2c, 31a, 31c
+12V	P1 pin 30a, P2 pin 30a
–12V	P1 pin 30b, P2 pin 30c

4.3 Serial Ports

The following table shows the CPU360 serial port connections on the 9 way D sockets in position S4. Port A uses the lower socket, and port B uses the upper socket.

Pin no.	Signal	Pin no.	Signal	
			RS-232	RS-485
1	High termination	6	CD	
2	TxD	7	RTS	/TxD
3	RxD	8	CTS	/RxD
4	Low termination	9		
5	0V			

Table 1: CPU360 serial port connections

The normal configuration in the PTS systems is for RS-232 signals on port A, the main terminal port, and RS-485 signals on port B for the Operator's Panel. The serial port transceivers are software controlled.

4.4 CANbus

The CPU360 has two double 9 way D plugs and sockets for two separate CANbus interfaces. Optional software will allow multiple PTS systems to be linked together via CANbus. This will support motor synchronisation between similar systems (peer to peer operation) and use of the CPU360 to supervise a number of CANbus slave modules. CAN interface 0 uses the plug and socket in the S5 position, while CAN interface 1 uses those in the S6 position. The plug and socket are connected pin-to-pin, to allow a simple daisy chain connection between several units using a standard cable assembly.

The connections for the CANbus interfaces on the front panel 9 way plugs and sockets are shown below. Note that these comply with the CAN in Automation (CiA) draft standard DS102 Version 2.0, CAN Physical Layer for Industrial Applications.

Pin no.	Signal	Pin no.	Signal
1	Reserved	6	GND
2	CAN_L	7	CAN_H
3	CAN_GND	8	ERROR
4	Reserved	9	CAN_V+ (7–13V)
5	CAN_SHLD (screen)		

Table 2: CANbus connections

Note that the CANbus interfaces require an external power supply to power the isolated network transceivers. This may be connected via any of the normal D type connectors, or it may be connected on the general purpose i/o connector P2. The CANbus power connections on P2 are as follows:

CAN0 V+ P2 pins 25a, 25c
CAN0 0V P2 pins 26a, 26c
CAN1 V+ P2 pins 27a, 27c
CAN1 0V P2 pins 28a, 28c

4.5 Daughter Board

Two additional 9 way D sockets are fitted to the CPU360 in position S3. These are provided for use by any optional daughter board. The lower D socket connects to daughter board socket XS5, and the upper D socket connects to daughter board socket XS3. Connections for these two sockets depend on the particular daughter board fitted.

The following table shows the external connections for the Bitbus interface daughter board on the 9 way D plug and socket in position S3. The Bitbus daughter board links the plug and socket together pin-to-pin to allow daisy chain cable connections.

Pin no.	Signal	Pin no.	Signal
1	Link1	6	Link6
2	GND	7	GND
3	DATA*	8	DATA
4	RTS*	9	RTS
5	RGND		

Table 3: Bitbus connections

Note that the Bitbus interface is fully isolated from the CPU360 power supplies.

4.6 Ethernet

The CPU360 provides an Ethernet interface using either a standard AUI port, or a twisted pair (10baseT) interface. The AUI port uses a standard 15 way D socket, and the twisted pair port uses an 8 way RJ-45 socket.

The pin functions for the AUI 15 way D socket are shown below.

Pin no.	Signal	Pin no.	Signal
1	GND	9	CL–
2	CL+	10	TX–
3	TX+	11	
4	GND	12	RX–
5	RX+	13	+12V
6	GND	14	GND
7		15	
8	GND		

Table 4: Ethernet AUI connections

4.7 G64 Bus

The connections to the G64 bus (P1) are given in this table.

Signal	Pin	Signal	Pin
0V supply GND	1a	0V supply GND	1b
Address line A0	2a	Address line A8	2b
Address line A1	3a	Address line A9	3b
Address line A2	4a	Address line A10	4b
Address line A3	5a	Address line A11	5b
Address line A4	6a	Address line A12	6b
Address line A5	7a	Address line A13	7b
Address line A6	8a	Address line A14	8b
Address line A7	9a	Address line A15	9b
Bus grant /BGT	10a	Bus request /BRQ	10b
Data strobe /DS0	11a	Data strobe /DS1	11b
	12a	Bus busy /BBUSY	12b
SYSCLK	13a	E clock	13b
Valid peripheral address /VPA	14a	Reset output /RESET	14b
MRDY or /DTACK	15a	Non-maskable interrupt /NMI	15b
Valid memory address /VMA	16a	Interrupt request /IRQ	16b
Read/write R/W	17a	Fast interrupt request /FIRQ	17b
	18a		18b
Data line /D8	19a	Data line /D12	19b
Data line /D9	20a	Data line /D13	20b
Data line /D10	21a	Data line /D14	21b
Data line /D11	22a	Data line /D15	22b
Data line /D0	23a	Data line /D4	23b
Data line /D1	24a	Data line /D5	24b
Data line /D2	25a	Data line /D6	25b
Data line /D3	26a	Data line /D7	26b
	27a		27b
Chain out CHOUT	28a	Chain in CHIN	28b
	29a		29b
+12V supply	30a	–12V supply	30b
+5V supply VCC	31a	+5V supply VCC	31b
0V supply GND	32a	0V supply GND	32b

Table 5: G64 bus connections : P1

4.8 General Purpose I/O

The general purpose input/output connections on plug P2 are given here.

Signal	Pin	Signal	Pin
0V supply GND	1a	0V supply GND	1c
+5V supply VCC	2a	+5V supply VCC	2c
Port line PA1	3a	Port line PA0	3c
Port line PA3	4a	Port line PA2	4c
Port line PA5	5a	Port line PA4	5c
Port line PA7	6a	Port line PA6	6c
Port line PC1	7a	Port line PC0	7c
Port line PC3	8a	Port line PC2	8c
0V	9a	0V	9c
Port line PB1	10a	Port line PB0	10c
Port line PB3	11a	Port line PB2	11c
Port line PB5	12a	Port line PB4	12c
Port line PB7	13a	Port line PB6	13c
Port line PC1	14a	Port line PC0	14c
Port line PC3	15a	Port line PC2	15c
0V	16a	0V	16c
	17a		17c
	18a		18c
	19a		19c
	20a		20c
	21a		21c
	22a		22c
	23a		23c
	24a		24c
CAN0 V+ (7-13V)	25a	CAN0 V+ (7-13V)	25c
CAN0 0V	26a	CAN0 0V	26c
CAN1V+ (7-13V)	27a	CAN1 V+ (7-13V)	27c
CAN1 0V	28a	CAN1 0V	28c
	29a		29c
+12V supply	30a	–12V supply	30c
+5V supply VCC	31a	+5V supply VCC	31c
0V supply GND	32a	0V supply GND	32c

Table 6: General purpose I/O connections : P2

4.9 Background Debug Port

The connections on the background debug connector P3 are given here. It is used during software development and testing.

Pin no.	Signal	Pin no.	Signal
1	/DS	2	/BERR
3	0V	4	/BKPT/DSCLK
5	0V	6	FREEZE
7	/RESET	8	IFETCH/DSI
9	+5V	10	IPIPE/DSO

Table 7: Background debug connector : P3

4.10 JTAG Port

The connections on the JTAG test connector P4 are given here. They are compatible with equipment supplied by JTAG Technologies BV. It is used during board testing.

Pin no.	Signal	Pin no.	Signal
1	/TRST	2	0V
3	TDO	4	0V
5	TDI	6	0V
7	TMS	8	0V
9	TCK	10	0V

Table 8: JTAG test connector : P4

Index

R

S

T

W

